承 认 书

SPECIFICATION FOR APPROVAL

客 户 名 称 （**Customer**）：

年　　月　　日

机种　　液晶显示模组

Machinery　　LCM

品名 ：　　VTM12232E2

Description

编号
No.

客 户 确 认 （APPROVED SIGNATURES）

上 海 恒 方 电 子有 限 公 司

SHANGHAI HENGFANG DISPLAY TECHNOLOGY LTD

本厂型号	**VTM12232E2**		
产品类型	液晶显示模组	送样日期	
修改次数	第 1 次	页 数	共 17 页
客户签回意见			

签名:

本承认书一式_____份,请签回一份给我方。

业 务	制 定	审 核	批 准

CONTENTS:

Revision record

Rev Mark	Revision description	Rev by	Rev date	Sample No
1.0	**Preliminary**	**JQY**	2009-9-29	**VTM12232E2**

1. FEATURES

VTM12232E2 is a low-power consumption dot matrix LCD module with built in controller. The controller has a built-in DDRAM. All the display functions are controlled by instructions and the module can be easily interfaced with an 8-bit 8080 parallel interface MPU.

1) Format: 122 x 32 Dots
2) Display type: STN(Y/G), transflective, Positive , 6 O'clock
3) Driving method: 1/32 duty, 1/6 bias.
4) Low power consumption.
5) Easy interfaced with a parallel interface MPU
6) Power supply Voltage:+5.0V
7) Yellow-green backlight voltage: DC 5.0V

2. MECHANICAL DATA

Item		Width	Height	Thickness	Unit
Module size without FFC		84	44	13	mm
Viewing area		60	18.5	—	mm
Dot	Size	0.4	0.4	—	mm
	Pitch	0.44	0.44	—	mm

3. MAXIMUN ABSOLUTE LIMIT

Item	Symbol	Test Condition	Standard Value			Unit
			Min.	Typ.	Max.	
Power Supply Voltage	Vdd -Vss	Ta=25℃	4.5	5.0	+5.5	V
Voltage Supply for LCD Drive	Vdd -Vo	Ta=25℃	—	5	7	V
Input Voltage	VI	Ta=25℃	-0.3	—	Vdd+0.3	V

4. TEMPERATUTE CHARACTERISTICS

Item	Symbol	Test Condition	Standard Value			Unit
			Min.	Typ.	Max.	
Operating Temperature	Topr	—	-10	—	+60	℃
Storage Temperature	Tstg	—	-20	—	+70	℃

5. ELECTRICAL CHARACTERISTICS

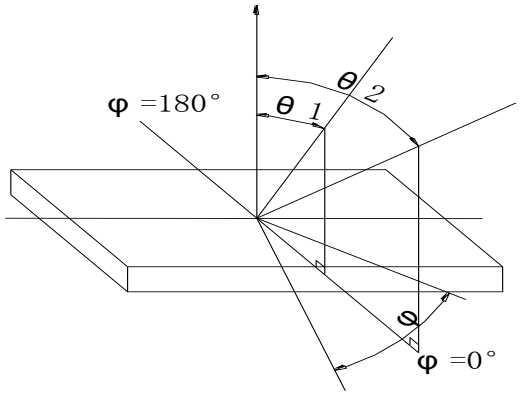
Item	Symbol	Condition	Standard value			Unit
			Min.	Typ	Max.	
Input "High" Voltage	V_{IH}	—	0.8Vdd	—	Vdd	V

Input “Low” Voltage	V_{IL}	—	0	—	0.2Vdd	V
Output “High” Voltage	V_{OH}	—	0.8Vdd	—	—	V
Output “Low” Voltage	V_{OL}	—	—	—	0.2Vdd	V

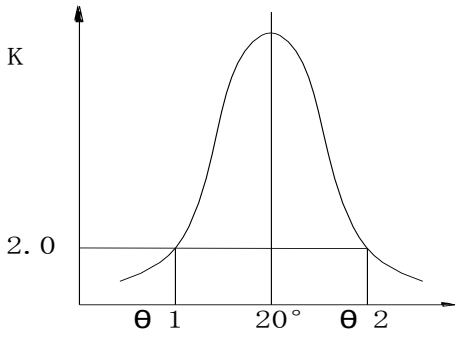
6. ELECTRO-OPTICAL CHARACTERISTICS

(Ta=25℃)

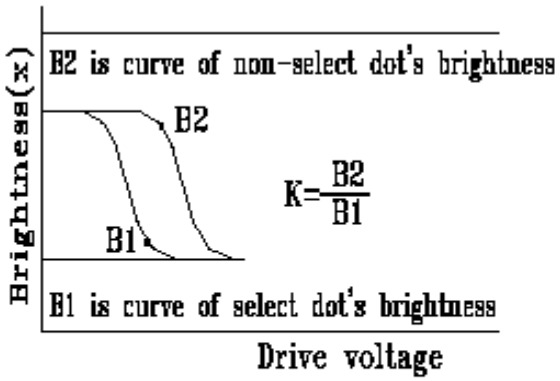
Item	Symbol	Condition	Min	Typ	Max	Unit
Contrast Ratio	K	ϕ =10°, θ=0°	4	5	—	-
Response Time (rise)	Tr	ϕ =10°, θ=0°	—	250	300	ms
Response Time(Fall)	Tf	ϕ=10°, θ=0°	—	300	350	ms
Viewing Angle	ϕ2-ϕ1	Kα=2	20	-	-	Deg.

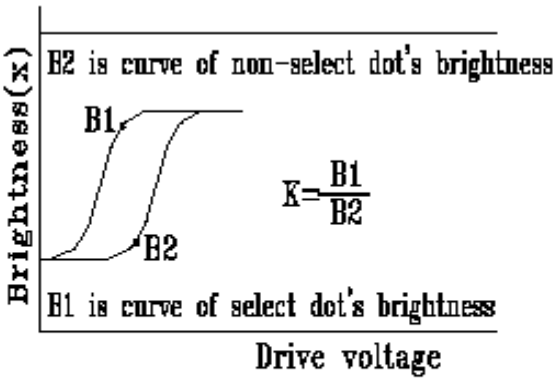


Positive Display



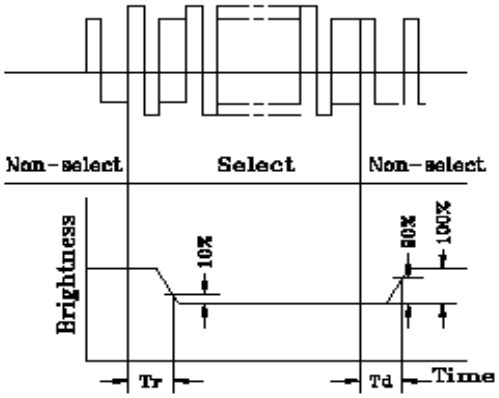
Negative Display



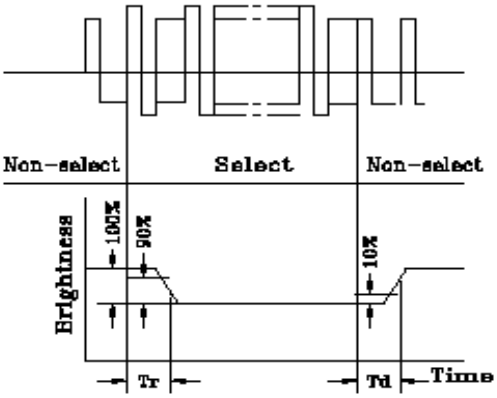


$$\text{Contrast Ratio (K)} \quad \frac{\text{Brightness of non-selected dot (B2)}}{\text{Brightness of selected dot (B1)}}$$

Positive Display



Negative Display



7. PIN CONNECTONS

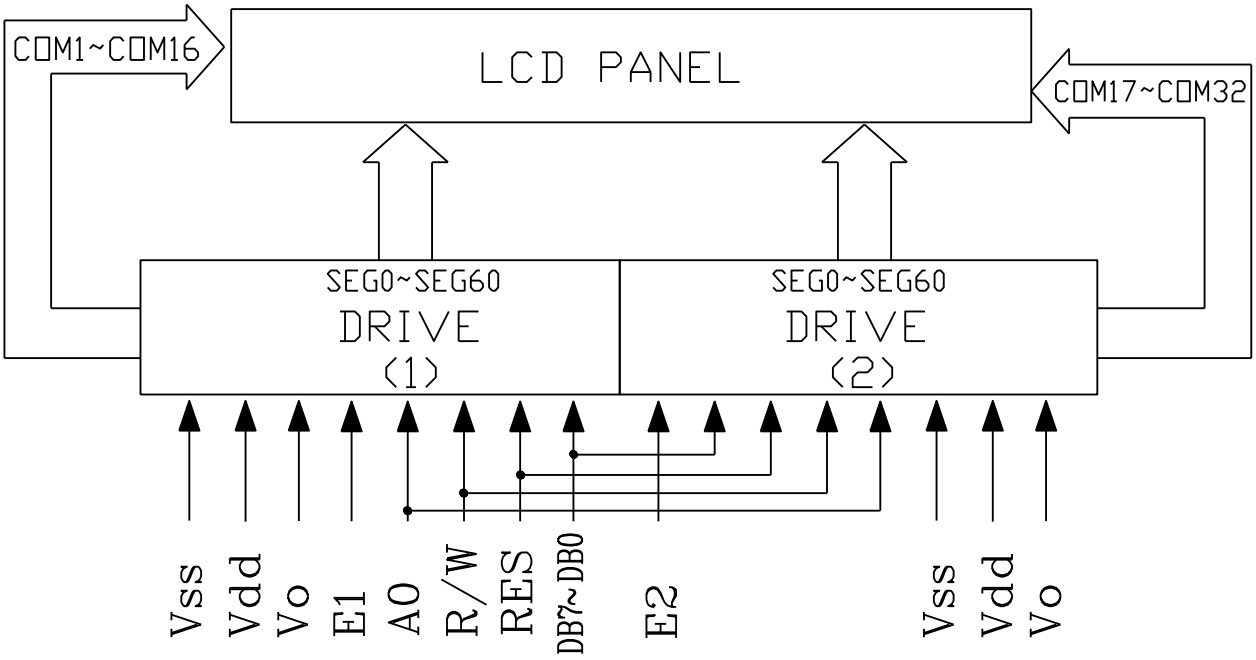
PIN NO.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
SYMBOL	VSS	VDD	Vo	A0	E1	E2	R/W	DB0	DB1	DB2	DB3	DB4	DB5	DB6	DB7	RES	A	K

PIN DESCRIPTION:

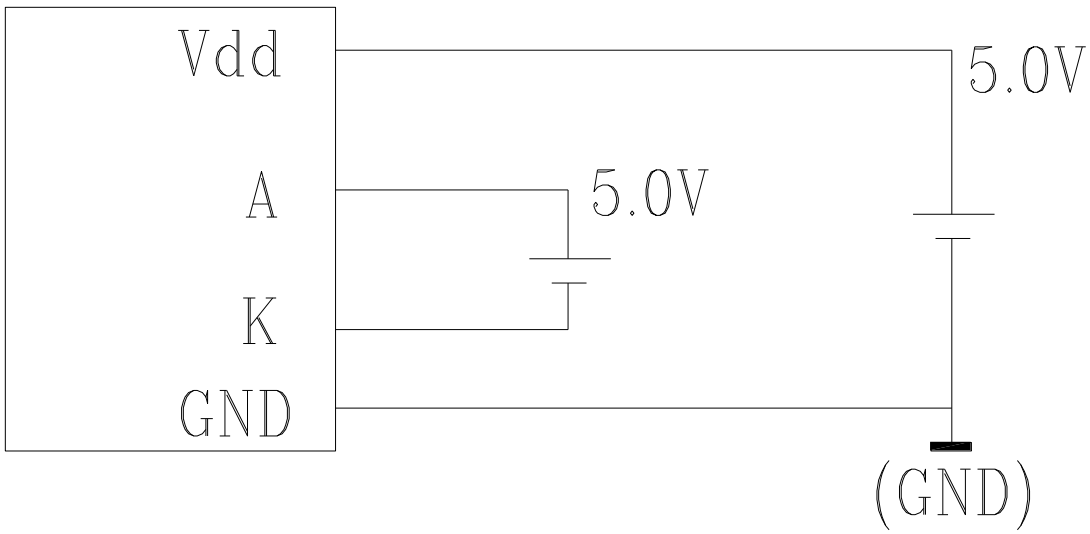
Pin No.	Pin Name	I/O	Description
1	VSS	-	Power ground.
2	VDD	-	Power supply for logic.
3	V0	-	Power supply for LCD driver circuit.
4	A0	I	DATA /COMMAND Control pin A0="H": Indicate that D0 to D7 are display data. A0="L": Indicates that D0 to D7 are control data.
5	E1	I	Chip 1 (U1)interfaced with 68 family MPU: Enable Clock signal input for the 68 family MPU. Chip interfaced with 80 family MPU: "L" Active input pin to which the 80 family MPU RD signal is connected. With this signal held at "L", the SED1520 data bus works as output.
6	E2	I	Chip 2 (U2)interfaced with 68 family MPU: Enable Clock signal input for the 68 family MPU. Chip interfaced with 80 family MPU: "L" Active input pin to which the 80 family MPU RD signal is connected. With this signal held at "L", the SED1520 data bus works as output.
7	R/W	I	Chip interface with 68 family MPU: Read/Write control signal input pin. R/W = "H" : Read R/W = "L" : Write Chip interfaced with 80 family MPU: "L" Active input pin to which the 80 family WR is connected. The signal on the data bus is fetched by the leading edge of WR.
9~16	DB0~DB7	I/O	8-bit data bus.

16	RES	I	Input pin. The SED1520 can be reset or initialized by setting RES to low level (if it is interfaced with a 68 family MPU) or high level (if with an 80 family MPU). This reset operation occurs when an edge of the RES signal is sensed. The level input selects the type of interface with the 68 or 80 family MPU: High level: Interface with 68 family MPU Low level: Interface with 80 family MPU
17	A	-	Anode of LED backlight
18	K	-	Cathode of LED backlight

8 BLOCK DIAGRAM

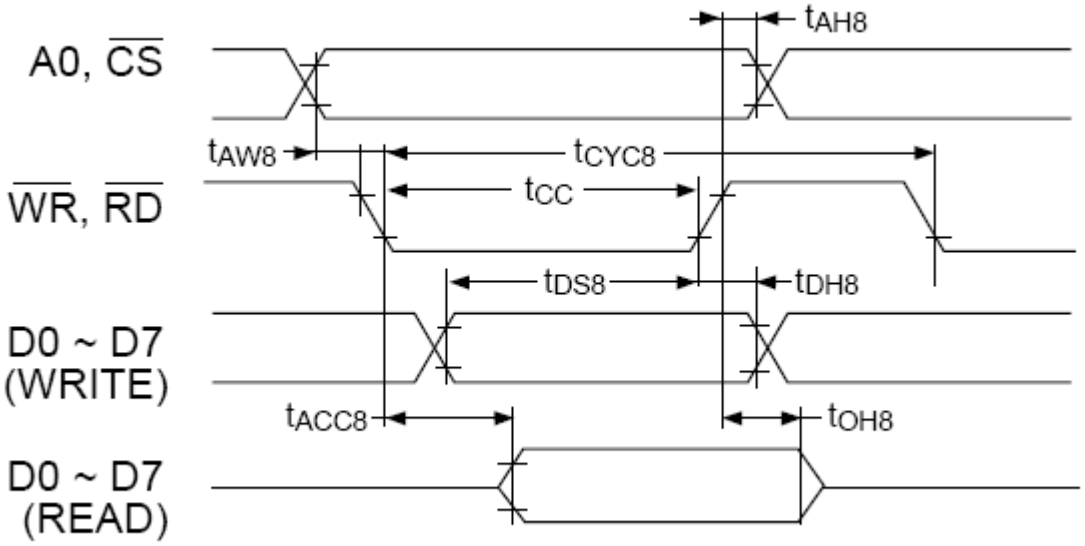


9. Power Supply



10. Bus Timing Characteristics

8080 family MPU

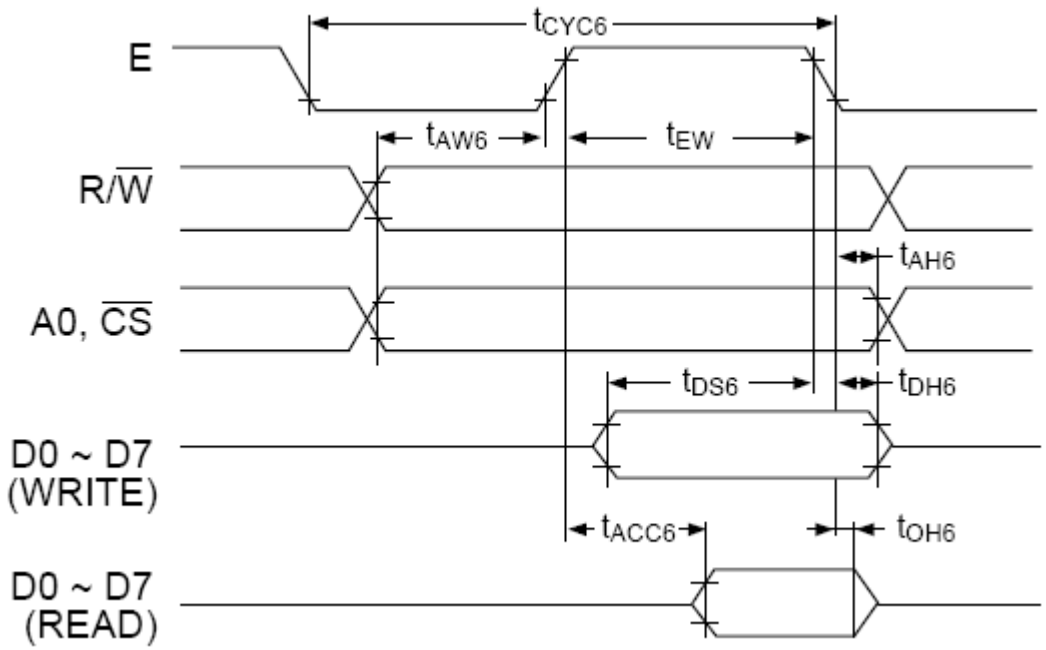


Ta = –20 to 75°C, VSS = –5.0V ± 10%, Unit: ns

Signal	Symbol	Parameter	Min.	Max.	Condition
A0, $\overline{CS}$	t AH8	Address hold time	10		
	t AW8	Address setup time	20		
$\overline{WR}$, $\overline{RD}$	t CYC8	System cycle time	1000		
	t CC	Control pulse width	200		
D0–D7	t DS8	Data setup time	80		
	t DH8	Data hold time	10		
	t ACC8	$\overline{RD}$ access time		90	CL = 100pF
	t OH8	Output disable time	10	60	

*1. Each of the values where VSS = –3.0V is about 200% of that where VSS = –5.0V (i.e., the listed value).
*2. The rise or fall time of input signals should be less than 15 ns.

6800 family MPU



Ta = –20 to 75°C, VSS = –5.0V ± 10%, Unit: ns

Signal	Symbol	Parameter		Min.	Max.	Condition
A0, CS R/W	t CYC6*1	System cycle time		1000		
	t AW6	Address setup time		20		
	t AH6	Address hold time		10		
D0–D7	t DS6	Data setup time		80		
	t DH6	Data hold time		10		
	tOH6	Output disable time		10	60	CL = 100pF
	t ACC6	Access time			90	
E	t EW	Enable pulse width	Read	100		
			Write	80		

*1. t CYC6 indicates the cycle time during which CS•E = "H". It does not mean the cycle time of signal E.

*2. Each of the values where VSS = –3.0V is about 200% of that where VSS = –5.0V (i.e., the listed value).

*3. The rise or fall time of input signals should be less than 15 ns.

11. INSTRUCTION SET

	Command	Code											Function
		A0	$\overline{RD}$	$\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
(1)	Display ON/OFF	0	1	0	1	0	1	0	1	1	1	0/1	Turns all display on or off, independently of display RAM data or internal status. 1: ON 0: OFF (Power-saving mode with static drive on)*
(2)	Display start line	0	1	0	1	1	0	Display Start Address (0–31)					Specifies RAM line corresponding to uppermost line (COM0) of display.
(3)	Set page address	0	1	0	1	0	1	1	1	0	Page (0–3)		Sets display RAM page in page address register.
(4)	Set column (segment) address	0	1	0	0	Column Address (0–79)							Sets display RAM column address in column address register.
(5)	Read status	0	0	1	Busy	ADC	ON/OFF	RESET	0	0	0	0	Reads the following status: BUSY 1: Internal operation, 0: Ready ADC 1: CW output (forward), 0: CCW output (reverse) ON/OFF 1: Display off, 0: Display on RESET 1: Being reset, 0: Normal
(6)	Write display data	1	1	0	Write Data								Writes data from data bus into display RAM. Display RAM location whose address has been preset is accessed. After access, the column address is incremented by 1.
(7)	Read display data	1	0	1	Read Data								Reads data from display RAM onto data bus.
(8)	Select ADC	0	1	0	1	0	1	0	0	0	0	0/1	Used to invert relationship of assignment between display RAM column addresses and segment driver outputs. 0: CW output (forward) 1: CCW output (reverse)
(9)	Static drive ON/OFF	0	1	0	1	0	1	0	0	1	0	0/1	Selects normal display or static driving operation. 1: Static drive (power-saving mode) 0: Normal driving
(10)	Select duty	0	1	0	1	0	1	0	1	0	0	0/1	Selects LCD cell driving duty. 1: 1/32 0: 1/16
(11)	Read modify write	0	1	0	1	1	1	0	0	0	0	0	Increments column address counter by 1 when display data is written. (This is not done when data is read.)
(12)	End	0	1	0	1	1	1	0	1	1	1	0	Clears read modify write mode.
(13)	Reset	0	1	0	1	1	1	0	0	0	1	0	Sets display start line register on the first line. Also sets column address counter and page address counter to 0.

Display ON/OFF

A_0	$\overline{RD}$	$R/\overline{W}$ $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	1	0	1	0	1	1	1	D	AEH, AFH

This command turns the display on and off.

- D=1: Display ON
- D=0: Display OFF

Display Start Line

This command specifies the line address shown in Figure 3 and indicates the display line that corresponds to COM0. The display area begins at the specified line address and continues in the line address increment direction. This area having the number of lines of the specified display duty is displayed. If the line address is changed dynamically by this command, the vertical smooth scrolling and paging can be used.

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	1	0	A4	A3	A2	A1	A0	C0H to DFH

This command loads the display start line register.

A4	A3	A2	A1	A0	Line Address
0	0	0	0	0	0
0	0	0	0	1	1
		:			:
		:			:
1	1	1	1	1	31

Set Page Address

This command specifies the page address that corresponds to the low address of the display data RAM when it is accessed by the MPU. Any bit of the display data RAM can be accessed when its page address and column address are specified. The display status is not changed even when the page address is changed.

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	0	1	1	1	0	A1	A0	B8H to BBH

This command loads the page address register.

A1	A0	Page
0	0	0
0	1	1
1	0	2
1	1	3

Set Column Address

This command specifies a column address of the display data RAM. When the display data RAM is accessed by the MPU continuously, the column address is incremented by 1 each time it is accessed from the set address. Therefore, the MPU can access to data continuously. The column address stops to be incremented at address 80, and the page address is not changed continuously.

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	0	A6	A5	A4	A3	A2	A1	A0	00H to 4FH

This command loads the column address register.

A6	A5	A4	A3	A2	A1	A0	Column Address
0	0	0	0	0	0	0	0
0	0	0	0	0	0	1	1
			:				:
			:				:
1	0	0	1	1	1	1	79

Read Status

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	BUSY	ADC	ON/OFF	RESET	0	0	0	0

Reading the command I/O register (A0=0) yields system status information.

- The busy bit indicates whether the driver will accept a command or not.
  Busy=1: The driver is currently executing a command or is resetting. No new command will be accepted.
  Busy=0: The driver will accept a new command.
- The ADC bit indicates the way column addresses are assigned to segment drivers.
  ADC=1: Normal. Column address n → segment driver n.
  ADC=0: Inverted. Column address 79-u → segment driver u.
- The ON/OFF bit indicates the current status of the display.
  It is the inverse of the polarity of the display ON/OFF command.
  ON/OFF=1: Display OFF
  ON/OFF=0: Display ON
- The RESET bit indicates whether the driver is executing a hardware or software reset or if it is in normal operating mode.
  RESET=1: Currently executing reset command.
  RESET=0: Normal operation

Write Display Data

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	Write data							

Writes 8-bits of data into the display data RAM, at a location specified by the contents of the column address and page address registers and then increments the column address register by one.

Read Display Data

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	Read data							

Reads 8-bits of data from the data I/O latch, updates the contents of the I/O latch with display data from the display data RAM location specified by the contents of the column address and page address registers and then increments the column address register.
After loading a new address into the column address register one dummy read is required before valid data is obtained.

Select ADC

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	0	1	0	0	0	0	D	A0H, A1H

This command selects the relationship between display data RAM column addresses and segment drivers.
D=1: SEG0 ← column address 4FH, … (inverted)
D=0: SEG0 ← column address 00H, … (normal)
This command is provided to reduce restrictions on the placement of driver ICs and routing of traces during printed circuit board design. See Figure 2 for a table of segments and column addresses for the two values of D.

Static Drive ON/OFF

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	0	1	0	0	1	0	D	A4H, A5H

Forces display on and all common outputs to be selected.
D=1: Static drive on
D=0: Static drive off

Select Duty

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	0	1	0	1	0	0	D	A8H, A9H

This command sets the duty cycle of the LCD drive and is only valid for the SED1520F and SED1522F. It is invalid for the SED1521F which performs passive operation. The duty cycle of the SED1521F is determined by the externally generated FR signal.

	SED1520	SED1522
D=1:	1/32 duty cycle	1/16 duty cycle
D=0:	1/16 duty cycle	1/8 duty cycle

When using the SED1520F0A, SED1522F0A (having a built-in oscillator) and the SED1521F0A continuously, set the duty as follows:

		SED1521D0A
SED1520D0A	1/32	1/32
	1/16	1/16

Read-Modify-Write

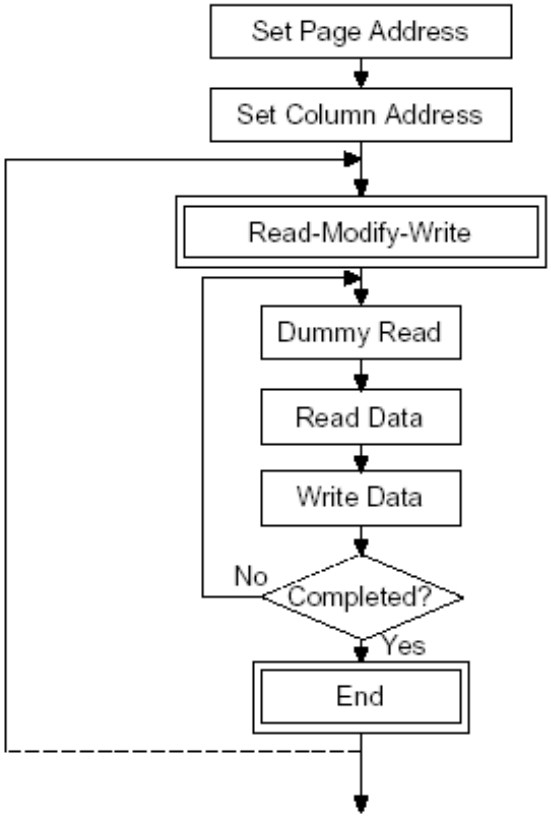
A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	1	1	0	0	0	0	0	E0H

This command defeats column address register auto-increment after data reads. The current conetents of the column address register are saved. This mode remains active until an End command is received.

- Operation sequence during cursor display

When the End command is entered, the column address is returned to the one used during input of Read-Modify-Write command. This function can reduce the load of MPU when data change is repeated at a specific display area (such as cursor blinking).

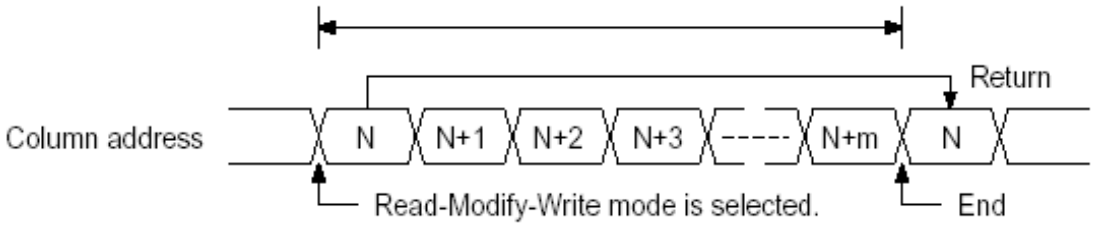
* Any command other than Data Read or Write can be used in the Read-Modify-Write mode. However, the Column Address Set command cannot be used.



End

A0	$\overline{RD}$	R/$\overline{W}$ $\overline{WR}$	D7	D6	D5	D4	D3	D2	D1	D0	
0	1	0	1	1	1	0	1	1	1	0	EEH

This command cancels read-modify-write mode and restores the contents of the column address register to their value prior to the receipt of the Read-Modify-Write command.



Reset

A_0	$\overline{RD}$	$R/\overline{W}$ $\overline{WR}$	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
0	1	0	1	1	1	0	0	0	1	0	E2H

This command clears
- the display start line register.
- and set page address register to 3 page.

It does not affect the contents of the display data RAM.
When the power supply is turned on, a Reset signal is entered in the $\overline{RES}$ pin. The Reset command cannot be used instead of this Reset signal.

Power Save (Combination command)

The Power Save mode is selected if the static drive is turned ON when the display is OFF. The current consumption can be reduced to almost the static current level. In the Power Save mode:
(a) The LCD drive is stopped, and the segment and common driver outputs are set to the V_{DD} level.
(b) The external oscillation clock input is inhibited, and the OSC2 is set to the floating mode.
(c) The display and operation modes are kept.
The Power Save mode is released when the display is turned ON or when the static drive is turned OFF. If the LCD drive voltage is supplied from an external resistance divider circuit, the current passing through this resistor must be cut by the Power Save signal.

12. RELIABILITY

- Reliability characteristics shall meet following requirements

ITEM	TEST	CRITERION
High temp	70℃/24HRS	* Total current consumption should be below double of initial value * Contrast ratio should be within initial value ±50% * No defect in cosmetic and operational function is allowable
Low temp	-20℃/24HRS	
High humidity	60℃×90%RH/24HRS	
Thermal shock	-20℃→25℃→70℃→/5 CYCLES (30min)(30min)(30min)	
Vibration	1 Operating time: thirty minutes exposure for each direction (x y z) 2 Sweep frequency (l min):10Hz→22HZ→10HZ 3 Amplitude:1.5mm	

13 PRECAUTIONS FOR USING

- HANDLING
  - Refrain from storing mechanical shock and from applying any force to LCD MODULE it may cause disoperation or damage of LCD
  - Do not touch ,press or rub the display panel with a hard, stiff tool or object as the polarizes in the panel are easily scratched
  - If LCD is broken and liquid crystal material flow out, ingestion, inhalation, or contact with skin should be avoided. If liquid crystal material contact with skin, wash immediately with alcohol and rinse thoroughly with water.
  - Never use organic solvents to clear the display panel as these solvent may adversely affect the polarizer. To clean the display panels dampen a bit of absorbent cotton with petroleum benzene and gently wipe the panel or contaminations by using a scotch tape.
  - Refrain from discharge of high electro-static voltage, it will damage C_MOS LSI in the MODULE

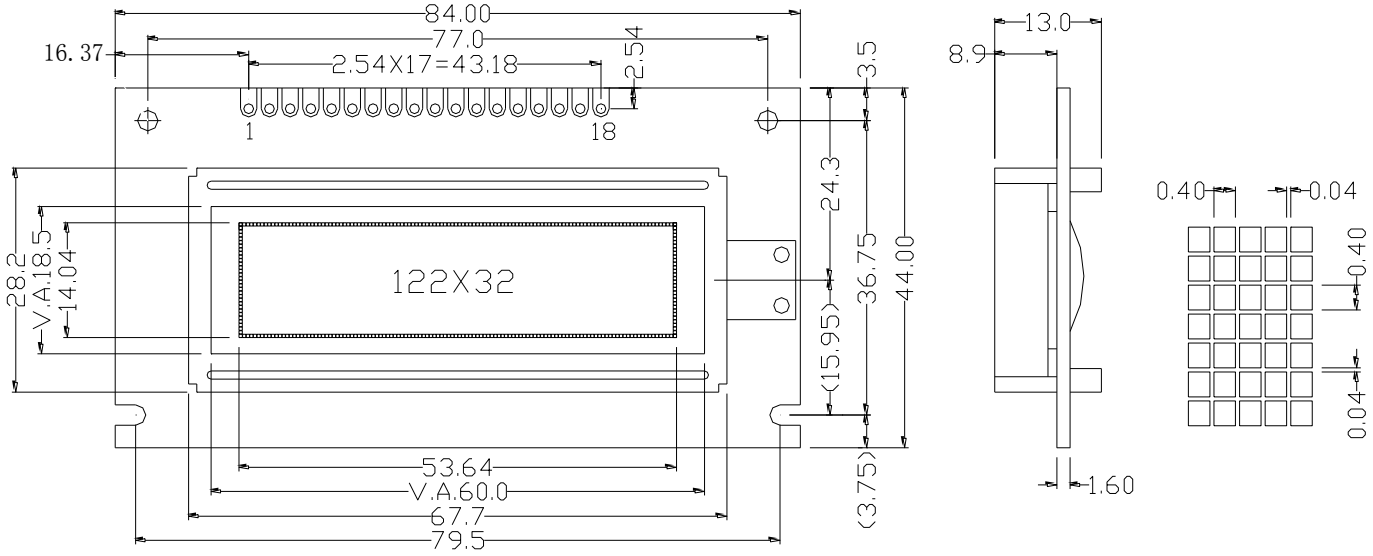
- Do not leave the MODULE in high temperature, especially in high humidity for a long time. It is recommended to store the MODULE where the temperature is in the range of 0℃ to 35℃ and the humidity is lower than 70%.
- Store the MODULE without exposure to direct sunlight or fluorescent lamp.
- Ultra violet cut filter is necessary for outdoor operation.
- Avoid condensation of water; it may cause disoperation or disconnection of electrode.

- OPERATION
  - Never connect or disconnect the LCD MODULE from the main system while power is being supplied.
  - When supplying the M signal from the external unit to a GRAPHIC MODULE, set the duty to 50% ± 1%.

If the duty deviates too greatly from the value, a DC voltage will be applied to the liquid crystal, which could induce an electrochemical reaction and reduce the life of the MODULE.

- Do not exceed the maximum rating values under the worst conditions taking account of the supply voltage variation, input voltage variation, and environmental temperature, etc. Otherwise LCD module may be damaged.

14 EXTERNAL DIMENSIONS



Unspecified tolerance is +/-0.3mm