Data International Co., Ltd.



APPROVAL SHEET

| Customer | : | |
|-------------|----|------------------------|
| Part Name | : | LCD MODULE |
| Model No. | :_ | DG-32240-27-SNCW-HCDTC |
| Drawing No. | :_ | |
| Approved by | :_ | |
| Date | : | |
| | | |

| Approved | Checked | Prepared | Sheet Code: |
|----------|---------|----------------|-------------|
| | | | |
| | | Ming-Chun Chen | 318-1053 |

CONTENTS

| 1. | SCO | PE | 3 |
|----|-------|--|--------|
| 2. | PRO | DUCT SPECIFICATIONS | 3 |
| | 2.1 | General | 3 |
| | 2.2 | Mechanical Characteristics | 3 |
| | 2.3 | Absolute Maximum Ratings | 4 |
| | 2.4 | Electrical Characteristics | 5 |
| | 2.5 | Optical Characteristics Absolute maximum ratings | 6 |
| | 2.6 | Optical Characteristics | 6 |
| | 2.7 | CCFL Back-light Characteristics | 9 |
| | 2.8 | Touch panel Specification | 10 |
| 3. | REL | IABILITY | 11 |
| 4. | OPE | RATING INSTRUCTIONS | 12 |
| | 4.1 | Input signal Function | 12 |
| | 4.2 | Voltage Generator Circuit | 13 |
| | 4.3 | Circuit Block Diagram | 14 |
| | 4.4 | Pin Description | 15 |
| | 4.5 | The Command Set | 16 |
| | 4.6 | Timing Characteristics | 17 |
| 5. | NOT | TES | 19 |
| 6. | OPE | RATION PRECAUTIONS | 19 |
| 7. | LCM | 1 DIMENSIONS | 20 |
| 8. | Instr | uction for touch panel | 21 |

DATA VISION 01/09/27 2 / 24

1. SCOPE

This specification covers the engineering requirements for the DGA-32240-27-SNCW-HCDTC liquid crystal module.

2. PRODUCT SPECIFICATIONS

2.1 General

• 320×240 dot matrix LCD

• STN (Blue mode)

• Negative, 6 o'clock, Wide temperature type

Back-light: CCFL, WhiteWith touch panel #9504

• Multiplexing driving: 1/240 duty, 1/14 bias

• Built-in controller 1335

2.2 Mechanical Characteristics

| Item | Characteristic |
|---|---------------------------------------|
| Dot configuration | 320×240 |
| Dot dimensions(mm) | 0.34×0.34 |
| Dot spacing (mm) | 0.02 |
| Module dimensions (Horizontal × Vertical × Thickness, mm) | $167.1 \times 109.0 \times 11.0$ max. |
| Viewing area (Horizontal × Vertical, mm) | 120.0×90.0 |
| Active area (Horizontal × Vertical, mm) | 115.17 × 86.37 |

DATA VISION 01/09/27 3 / 24

2.3 Absolute Maximum Ratings (Without CCFL back-light)

Absolute Maximum Ratings

| Parameter | Symbol | Rating | Unit |
|---|---------|-------------------|------|
| Supply voltage range | VDD | -0.3 to 7.0 | V |
| Input voltage range | VIN | -0.3 to VDD + 0.3 | V |
| Power dissipation | PD | 300 | mW |
| Operating temperature range | Topg | -20 to 75 | °C |
| Storage temperature range | Tstg | -65 to 150 | °C |
| Soldering temperature (10 seconds). See note 1. | Tsolder | 260 | °C |

Notes:

- 1. The humidity resistance of the flat package may be reduced if the package is immersed in solder. Use a soldering technique that does not heatstress the package.
- 2. If the power supply has a high impedance, a large voltage differential can occur between the input and supply voltages. Take appropriate care with the power supply and the layout of the supply lines. (See section 6.2.)
- 3. All supply voltages are referenced to Vss = 0V.

DATA VISION 01/09/27 4 / 24

2.4 Electrical Characteristics (Without CCFL back-light)

 $VDD = 4.5 \text{ to } 5.5V, VSS = 0V, Ta = -20 \text{ to } 75^{\circ}C$

| Parameter | Cumbal | Condition | | Unit | | |
|---------------------------------|--------|--|-----------|--------|-----------|------|
| Parameter | Symbol | Condition | min | typ | max | Onit |
| Supply voltage | VDD | | 4.5 | 5.0 | 5.5 | V |
| Register data retention voltage | Vон | | 2.0 | _ | 6.0 | V |
| Input leakage current | ILI | VI = VDD. See note 5. | _ | 0.05 | 2.0 | μΑ |
| Output leakage current | ILO | VI = VSS. See note 5. | _ | 0.10 | 5.0 | μΑ |
| Operating supply current | lopr | See note 4. | _ | 11 | 15 | mA |
| Quiescent supply current | IQ | Sleep mode, $V_{OSC1} = V_{\overline{CS}} = V_{\overline{RD}} = V_{DD}$ | _ | 0.05 | 20.0 | μΑ |
| Oscillator frequency | fosc | Measured at crystal, | 1.0 | _ | 10.0 | MHz |
| External clock frequency | fCL | 47.5% duty cycle. | 1.0 | _ | 10.0 | MHz |
| Oscillator feedback resistance | Rf | See note 6. | 0.5 | 1.0 | 3.0 | МΩ |
| TTL | | | | | | |
| HIGH-level input voltage | VIHT | See note 1. | 0.5VDD | _ | VDD | V |
| LOW-level input voltage | VILT | See note 1. | Vss | _ | 0.2VDD | V |
| HIGH-level output voltage | Vонт | Іон = -5.0 mA. See note 1. | 2.4 | _ | _ | V |
| LOW-level output voltage | Volt | IoL = 5.0 mA. See note 1. | _ | _ | Vss + 0.4 | V |
| CMOS | | | | | | |
| HIGH-level input voltage | VIHC | See note 2. | 0.8Vpp | _ | VDD | V |
| LOW-level input voltage | VILC | See note 2. | Vss | _ | 0.2VDD | V |
| HIGH-level output voltage | Vонс | Iон = −2.0 mA. See note 2. | VDD - 0.4 | _ | _ | V |
| LOW-level output voltage | Volc | Iон = 1.6 mA. See note 2. | _ | _ | Vss + 0.4 | V |
| Open-drain | | | | | | |
| LOW-level output voltage | Voln | IoL = 6.0 mA. | | | Vss + 0.4 | V |
| Schmitt-trigger | | <u> </u> | | | | |
| Rising-edge threshold voltage | VT+ | See note 3. | 0.5VDD | 0.7VDD | 0.8VDD | V |
| Falling-edge threshold voltage | VT- | See note 3. | 0.2VDD | 0.3VDD | 0.5VDD | V |

Notes:

- 1. D0 to D7, A0, $\overline{\text{CS}}$, $\overline{\text{RD}}$, $\overline{\text{WR}}$, VD0 to VD7, VA0 to VA15, $\overline{\text{VRD}}$, $\overline{\text{VWR}}$ and $\overline{\text{VCE}}$ are TTL-level inputs.
- 2. SEL1 is CMOS-level inputs. YD, XD0 to XD3, XSCL, LP, WF, YDIS are CMOS-level outputs.
- 3. RES is a Schmitt-trigger input. The pulsewidth on RES must be at least 200 µs. Note that pulses of more than a few seconds will cause DC voltages to be applied to the LCD panel.
- 4. fosc = 10 MHz, no load (no display memory), internal character generator, 256 × 200 pixel display. The operating supply current can be reduced by approximately 1 mA by setting both CLO and the display OFF.
- 5. VD0 to VD7 and D0 to D7 have internal feedback circuits so that if the inputs become high-impedance, the input state immediately prior to that is held. Because of the feedback circuit, input current flow occurs when the inputs are in an intermediate state.
- 6. Because the oscillator circuit input bias current is in the order of μA , design the printed circuit board so as to reduce leakage currents.

DATA VISION 01/09/27 5 / 24

2.5 Optical Characteristics Absolute maximum ratings

| Item | Symbol | Rating | Unit |
|-----------------------------|--------|--------|------|
| Operating temperature range | Тор | -20~70 | °C |
| Storage temperature range | Tst | -30~80 | °C |

2.6 Optical Characteristics

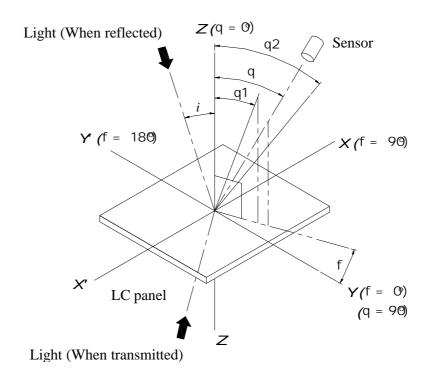
1/240 duty, 1/14 bias

| Item | Symbol | Temp. | Min. | Тур. | Max. | Unit | |
|-----------------|-----------------|-------|------|------|------|------|--|
| | | 0°C | 23.6 | 24.3 | 25.0 | | |
| Driving voltage | Vop | 25°C | 22.8 | 23.5 | 24.2 | V | |
| voltage | | 50°C | 21.9 | 22.6 | 23.3 | | |
| Contrast | CD | θ=0° | 4.3 | 5.4 | | | |
| ratio | CR | φ=0° | 7.5 | 3.4 | | | |
| Frame freq. | fF | | | 70 | | Hz | |
| Viewing | Θ_1 | | | 43 | | deg. | |
| angle* | θ_2 | 25°C | | 29 | | ueg. | |
| Response | t _{on} | 25°C | | 157 | | ms | |
| time | $t_{ m off}$ | 23 C | | 255 | | 1118 | |

DATA VISION 01/09/27 6 / 24

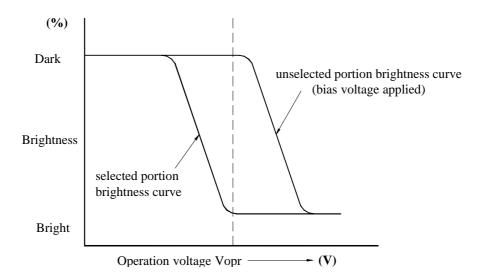
2.6.1 Definition of optical characteristics

*Definition of angles ϕ and θ



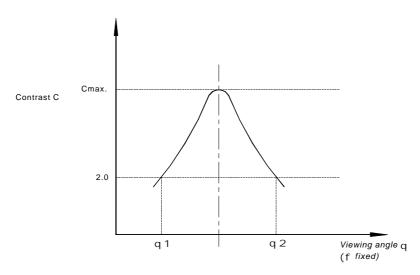
*Definition of contrast C

$$C = \frac{B1}{B2} = \frac{\text{Brightness of selected portion}}{\text{Brightness of unselected portion}}$$



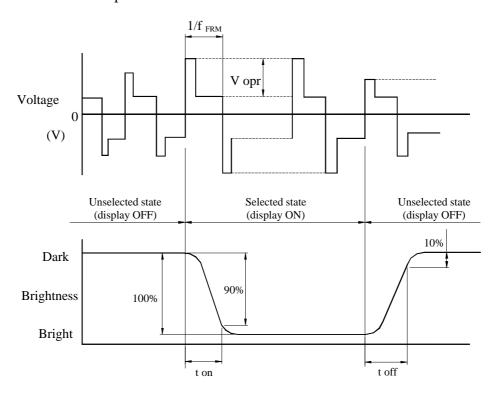
DATA VISION 01/09/27 7 / 24

*Definition of viewing angles $\theta 1$ and $\theta 2$



Note : Optimum vision with the naked eye and viewing angle θ at Cmax above are not always the same.

*Definition of response time



Vop : Operating voltage (V) ton : Response time (rise) (ms)

fFRM : Frame frequency (Hz) toff : Response time (fall) (ms)

DATA VISION 01/09/27 8 / 24

2.7 CCFL Electrical Specifications

2.7.1 Absolute maximum Conditions

The half-brightness life of the back light shall be kept as specified under the following absolute maximum conditions.

1.35W

Power Consumption

Ta=25°C, fL=55KHz

Tube current

Ta=25°C, fL=55KHz 5.0 ± 1.0 mArms max.

2.7.2 Electrical characteristics

The following operating conditions are recommended for the back light unit.

Start Voltage 630Vrms at Ta=25°C Tube Voltage 270Vrms at Ta=25°C Tube Current 5.0±0.5mArms at Ta=25°C Trive frequency 60±35KHz typ at Ta=25°C

2.7.3 Initial Optical Characteristics

The unit shall satisfy the following criteria at 25±2°C ambient temperature, 45%-85% relative humidity, no air flow and with applying rating input voltage and input current by using TDK L10L inverter.

Brightness Uniformity 75%

Average Brightness 550cd/m² min. at Ta=25°C

(Measurement shall be continuous on for 30 minutes)

Chromaticity $x=0.3475\pm0.0015$

 $y=0.3750\pm0.0005$

2.7.4 Life

the unit shall satisfy the following criteria at 25±5°C ambient temperature, with 5mA tube current by using TDK L10L inverter.

Half-Brightness Life of Unit

15,000 Hours min.

The definition of half-brightness life is either average brightness reach to 50% of initial average brightness or lamp stopping light emission.

2.7.5 Operating Conditions

Temperature 0 to 50°C Humidity 30 to 85% RH

2.7.6 Storage Conditions

Temperature -20 to 80°C Humidity 5 to 90% RH

DATA VISION 01/09/27 9 / 24

2.8 Touch panel Specification

2.8.1 Typical Optical characteristics

- Visible Light Transmission : >80% @550nm.
- Haze: $5\%\pm2\%$ through hard coated PET only
- Operation temperature

From -10°C to 50°C (Humidity: 90% RH)

• Storage temperature

From -20°C to 70°C (At Ambient Humidity)

2.8.2 Electrical

• Operating Voltage : 5.5V or less

• Contact current : 20mA(maximum)

• Circuit close resistance : X : 650±200W

Y: 300±200W

• Circuit open resistance : >20M Ω at 25VDC

• Contact bounce : <15ms

• Linear Test: ±1.5% or Less

2.8.3 Linearity

• Linear Test Specification:

Direction X : -1.5% or less

Direction $Y : \pm 1.5\%$ or less

• Line Test Circuit for Y Coordinate

Add 5V between Y1 and Y2, touch the point C0R0 to C9R9 separately, and measure the voltage from X1.

DATA VISION 01/09/27 10 / 24

3. RELIABILITY

3.1 Reliability

| Test item | Test condition | Evaluation and assessment |
|--|---|---|
| Operation at high temperature and humidity | 40°C±2°C 90%RH for 500hours | No abnormalities in functions* and appearance** |
| Operation at high temperature | 60°C±2°C for 500 hours | No abnormalities in functions* and appearance** |
| Heat shock | -20± ~ +60 °C Left for 1 hour at each temperature, transition time 5 min, repeated 10times | No abnormalities in functions* and appearance** |
| Low temperature | -20±2 °C for 500 hours | No abnormalities in functions* and appearance** |
| Vibration | Sweep for 1 min at 10 Hz, 55Hz, 10Hz, amplitude 1.5mm 2 hrs each in the X,Y and Z directions | No abnormalities in functions* and appearance** |
| Drop shock | Dropped onto a board from a height of 10cm | No abnormalities in functions* and appearance** |

^{*} Dissipation current, contrast and display functions

3.2 Liquid crystal panel service life

100,000 hours minimum at 25 °C±10 °C

- 3.3 Definition of panel service life
 - Contrast becomes 30% of initial value
 - Current consumption becomes three times higher than initial value
 - Remarkable alignment deterioration occurs in LCD cell layer
 - Unusual operation occurs in display functions

DATA VISION 01/09/27 11 / 24

^{**} Polarizing filter deterioration, other appearance defects

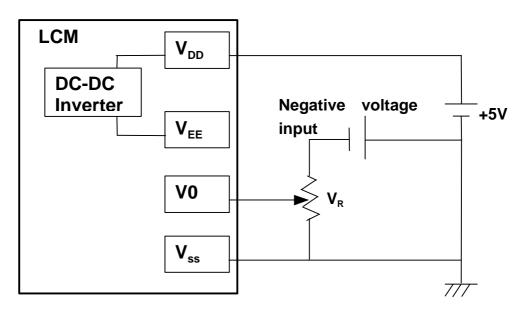
4. OPERATING INSTRUCTIONS

4.1 Input signal Function

| NO. | Symbol | Function |
|------|---------|--|
| 1 | VSS | Ground (0V) |
| 2 | VDD | Power supply for Logic circuit (+) |
| 3 | V0 | Power supply for LCD Contrast adjustment |
| 4 | A0 | Data Type Selection |
| 5 | /WR | 80 Series: Read Signal |
| | | 68 Series: Enable Signal(E) |
| 6 | /RD | 80 Series: Read Signal |
| | | 68 Series: Enable Signal(E) |
| 7~14 | DB0~DB7 | Display Data |
| 15 | /CS | Chip select Signal |
| 16 | /RESET | Rest Signal |
| 17 | VEE/NC | Power supply for LCD driving / NC |
| 18 | SEL1 | 8080or6800 family interface select |
| 19 | DCLK | External Clock Input. This clock runs the SAR conversion process and |
| | | synchronizes serial data I/O. |
| 20 | /CS | Chip Select Input.Controls conversion timing and enables the serial input/output |
| | | register. |
| 21 | DIN | Serial Data Input. If CS is LOW, data is latched on rising edge of DCLK. |
| 22 | DOUT | Serial Data Output. Data is shifted on the falling edge of DCLK. This output is |
| | | high impedance when CS is High. |
| 23 | PEN | Pen interrupt. |
| 24 | PEN1 | Pen interrupt setting. |
| 25 | IN3 | Auxiliary Input 1. ADC input Channel 3. |
| 26 | IN4 | Auxiliary Input 2. ADC input Channel 4. |

DATA VISION 01/09/27 12 / 24

4.2 Voltage Generator Circuit



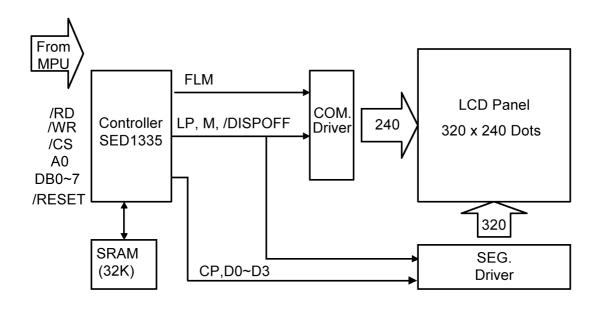
 V_R : 10K~20K Ohms

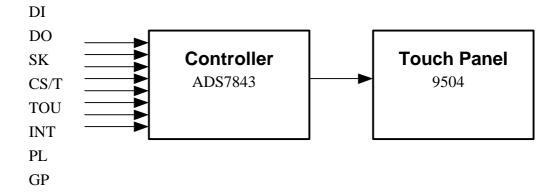
LCM :Built-in DC-DC inverter



DATA VISION 01/09/27 13 / 24

4.3 Circuit Block Diagram





DATA VISION 01/09/27 14 / 24

4.4 Pin Description

| Nama | Nun | nber | T | Description | | |
|-------------|----------------------|--------------------|--------------|---|--|--|
| Name | SED1335F0A | SED1335F0B | Туре | Description | | |
| VA0 to VA15 | 27 to 28 30 to 43 | 1 to 6 50 to 59 | Output | VRAM address bus | | |
| VWR | 44 | 7 | Output | VRAM write signal | | |
| VCE | 45 | 8 | Output | Memory control signal | | |
| VRD | 46 | 9 | Output | VRAM read signal | | |
| RES | 47 | 10 | Input | Reset | | |
| NC | 28, 48, 49 | 11, 12, 60 | _ | No connection | | |
| RD | 50 | 13 | Input | 8080 family: Read signal 6800 family: Enable clock (E) | | |
| WR | 51 | 14 | Input | 8080 family: Write signal 6800 family: R/W signal | | |
| SEL2 | 52 | 15 | Input | 8080 or 6800 family interface select | | |
| SEL1 | 53 | 16 | Input | 8080 or 6800 family interface select | | |
| XG | 54 | 17 | Input | Oscillator connection | | |
| XD | 55 | 18 | Output | Oscillator connection | | |
| <u>CS</u> | 56 | 19 | Input | Chip select | | |
| A0 | 57 | 20 | Input | Data type select | | |
| VDD | 58 | 21 | Supply | 2.7 to 5.5V supply | | |
| D0 to D7 | 59 to 60 1 to 6 | 22 to 29 | Input/output | Data bus | | |
| XD0 to XD3 | 7 to 10 | 30 to 33 | Output | X-driver data | | |
| XECL | 11 | 34 | Output | X-driver enable chain clock | | |
| XSCL | 12 | 35 | Output | X-driver data shift clock | | |
| Vss | 13 | 36 | Supply | Ground | | |
| LP | 14 | 37 | Output | Latch pulse | | |
| WF | 15 | 38 | Output | Frame signal | | |
| YDIS | 16 | 39 | Output | Power-down signal when display is blanked | | |
| YD | 17 | 40 | Output | Scan start pulse | | |
| YSCL | 18 | 41 | Output | Y-driver shift clock | | |
| VD0 to VD7 | 19 to 26 | 42 to 49 | Input/output | VRAM data bus | | |

DATA VISION 01/09/27 15 / 24

4.5 The Command Set

| Class Command | | | Code | | | | | | | | | Hex | Command Description | Command Read Parameters | | |
|----------------|-------------|----|------|----|----|----|------------|----|----|----|---------|---------|---------------------|---|-----------------|--------------|
| | | RD | WR | A0 | D7 | D6 | D 5 | D4 | D3 | D2 | D1 | D0 | | - | No. of Bytes | Sec- tion |
| System control | SYSTEM SET | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 40 | Initialize device and display | 8 | 8.2.1 |
| Control | SLEEP IN | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 53 | Enter standby mode | 0 | 8.2.2 |
| | DISP ON/OFF | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | D | 58, 59 | Enable and disable display and display flashing | 1 | 8.3.1 |
| | SCROLL | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 44 | Set display start address and display regions | 10 | 8.3.2 |
| | CSRFORM | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 5D | Set cursor type | 2 | 8.3.3 |
| Display | CGRAM ADR | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 5C | Set start address of character generator RAM | . 2 | 8.3.6 |
| control | CSRDIR | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | CD 1 | CD 0 | 4C to 4F | Set direction of cursor movement | 0 | 8.3.4 |
| | HDOT SCR | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 5A | Set horizontal scroll position | 1 | 8.3.7 |
| | OVLAY | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 5B | Set display overlay format | 1 | 8.3.5 |
| Drawing | CSRW | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 46 | Set cursor address | 2 | 8.4.1 |
| control | CSRR | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 47 | Read cursor address | 2 | 8.4.2 |
| Memory | MWRITE | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 42 | Write to display memory | | 8.5.1 |
| control | MREAD | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 43 | Read from display memory | _ | 8.5.2 |

Notes:

- a. CSRW, CSRR: Each byte is processed individually. The microprocessor may read or write just the low byte of the cursor address.
- b. SYSTEM SET, SCROLL, CGRAM ADR: Both parameter bytes are processed together. If the command is changed after half of the parameter has been input, the single byte is ignored.
- 2. APL and APH are 2-byte parameters, but are treated as two 1-byte parameters.

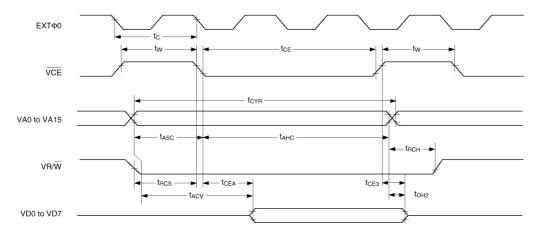
DATA VISION 01/09/27 16 / 24

^{1.} In general, the internal registers of the SED1335 series are modified as each command parameter is input. However, the microprocessor does not have to set all the parameters of a command and may send a new command before all parameters have been input. The internal registers for the parameters that have been input will have been changed but the remaining parameter registers are unchanged.

²⁻byte parameters (where two bytes are treated as 1 data item) are handled as follows:

4.6 Timing Characteristics

Display memory read timing

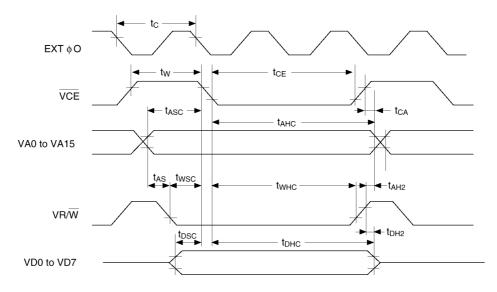


 $Ta = -20 \text{ to } 75^{\circ}\text{C}$

| Signal | Symbol | Parameter | VDD = 4.5 to 5.5V | | VDD = 2.7 to 4.5V | | 11 | 0 |
|----------------|--------|--|-------------------|-----------|-------------------|-----------|------|----------------|
| | | | min | max | min | max | Unit | Condition |
| EXT $\phi 0$ | tC | Clock period | 100 | _ | 125 | _ | ns | CL = 100 pF |
| VCE | tw | VCE HIGH-level pulsewidth | tc - 50 | _ | tc - 50 | _ | ns | |
| | tce | VCE LOW-level pulsewidth | 2tc - 30 | _ | 2tc - 30 | _ | ns | |
| VA0 to VA15 | tcyr | Read cycle time | 3tc | _ | 3tC | _ | ns | |
| | tasc | Address setup time to falling edge of VCE | tc - 70 | _ | tc - 100 | _ | ns | |
| | tahc | Address hold time from falling edge of VCE | 2tc - 30 | _ | 2tc - 40 | _ | ns | |
| VRD | tRCS | Read cycle setup time to falling edge of $\overline{\text{VCE}}$ | tc - 45 | _ | tc - 60 | _ | ns | |
| | trch | Read cycle hold time from rising edge of VCE | 0.5tC | _ | 0.5tC | _ | ns | |
| VD0 to VD7 | tACV | Address access time | _ | 3tc - 100 | _ | 3tC - 115 | ns | |
| | tCEA | VCE access time | _ | 2tc - 80 | _ | 2tc - 90 | ns | |
| | tOH2 | Output data hold time | 0 | _ | 0 | _ | ns | |
| | tCE3 | VCE to data off time | 0 | _ | 0 | _ | ns | |

DATA VISION 01/09/27 17 / 24

Display memory write timing



 $Ta = -20 \text{ to } 75^{\circ}C$

| Signal | Symbol | Parameter | VDD = 4.5 to 5.5V | | VDD = 2.7 to 4.5V | | Unit | Condition |
|----------------|--------|---|-------------------|-----|-------------------|-----|------|----------------|
| | | | min | max | min | max | Unit | Condition |
| EXT ϕ 0 | tC | Clock period | 100 | _ | 125 | _ | ns | CL = 100 pF |
| VCE | tw | VCE HIGH-level pulsewidth | tc - 50 | _ | tc - 50 | _ | ns | |
| | tCE | VCE LOW-level pulsewidth | 2tc - 30 | _ | 2tc - 30 | _ | ns | |
| VA0 to VA15 | tcyw | Write cycle time | 3tC | _ | 3tC | _ | ns | |
| | tAHC | Address hold time from falling edge of VCE | 2tc - 30 | _ | 2tc - 40 | _ | ns | |
| | tasc | Address setup time to falling edge of VCE | tc - 70 | _ | tc - 110 | _ | ns | |
| | tCA | Address hold time from rising edge of VCE | 0 | _ | 0 | _ | ns | |
| | tAS | Address setup time to falling edge of VWR | 0 | _ | 0 | _ | ns | |
| | tAH2 | Address hold time from rising edge of VWR | 10 | _ | 10 | _ | ns | |
| VWR | twsc | Write setup time to falling edge of VCE | tc - 80 | _ | tc – 115 | _ | ns | |
| | twnc | Write hold time from falling edge of VCE | 2tc - 20 | _ | 2tc - 20 | _ | ns | |
| VD0 to VD7 | tDSC | Data input setup time to falling edge of VCE | tc – 85 | | tc – 125 | _ | ns | |
| | tDHC | Data input hold time from falling edge of VCE | 2tc - 30 | _ | 2tc - 30 | _ | ns | |
| | tDH2 | Data hold time from rising edge of VWR | 5 | 50 | 5 | 50 | ns | |

Note: VD0 to VD7 are latching input/outputs. While the bus is high impedance, VD0 to VD7 retain the write data until the data read from the memory is placed on the bus.

DATA VISION 01/09/27 18 / 24

5. NOTES

<u>Safety</u>

• If the LCD panel breaks, be careful not to get the liquid crystal in your mouth. If the liquid crystal touches your skin or clothes, wash it off immediately using soap and plenty of water.

Handling

- Avoid static electricity as this can damage the CMOS LSI.
- The LCD panel is plate glass; do not hit or crush it.
- Do not remove the panel or frame from the module.
- The polarizing plate of the display is very fragile; handle it very carefully

Mounting and Design

- Mount the module by using the specified mounting part and holes.
- To protect the module from external pressure, leave a small gap by placing transparent plates (e.g. acrylic or glass) on the display surface, frame, and polarizing plate
- Design the system so that no input signal is given unless the power-supply voltage is applied.
- Keep the module dry. Avoid condensation, otherwise the transparent electrodes may break.

Storage

- Store the module in a dark place where the temperature is 25 °C±10 °C and the humidity below 65% RH.
- Do not store the module near organic solvents or corrosive gases.
- Do not crush, shake, or jolt the module (including accessories).

Cleaning

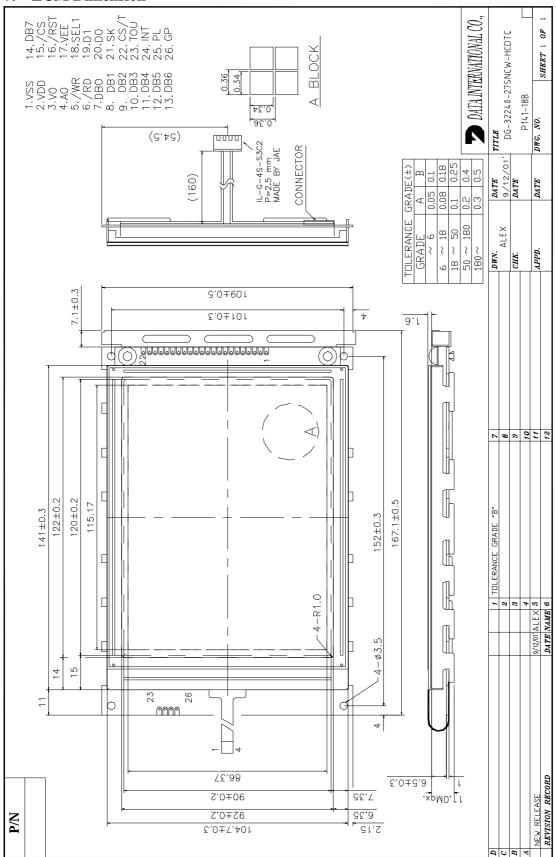
- Do not wipe the polarizing plate with a dry cloth, as it may scratch the surface.
- Wipe the module gently with soft cloth soaked with a petroleum benzine.
- Do not use ketonic solvents (ketone and acetoe) or aromatic solvents (toluene and xylene), as they may damage the polarizing plate.

6. OPERATION PRECAUTIONS

Any changes that need to be made in this specification or any problems arising from it will be dealt with quickly by discussion between both companies.

DATA VISION 01/09/27 19 / 24

7. LCM Dimension



DATA VISION 01/09/27 20 / 24

8. Instruction for touch panel

Following precaution should be taken on use of Touch Screen (ITO resistive analog detective type and matrix detective type.)

8.1 PRECAUTION ON DESIGNING TOUCH PANEL

(Please see touch panel plane drawing 1.)

8.1.1 ACTIVE AREA

Active area is described as inputted area by pen or finger, which assures quality clarified on the specifications related to input action such as functional property, optical property and durability.

- For detection of coordinates and calibration, it should be always conducted within active area. If it is conducted outside of the active area, it may cause functional error.
- Area, which is actually inputted by pen of finger, should be designed within active area. If it is designed outside of the active area, it may cause functional error.

8.1.2 NEUTRAL AREA

Neutral area is located in outside of the active area by 0.2~1.0mm (inside of non active area by 0.2~1.0mm), coordinated can be detected, but its location is in outside of the area which assures quality clarified on specifications related to input action such as functional property, optical property and durability.

Functional property, optical property and durability.

- Neural area detects coordinates when inputted by pen or finger, but it may cause functional error when it is transacted as data detected.
- Since a role of the neutral area is to protect non-active area, hard pushing by tip of a pen, etc. may cause deterioration of its durability.

8.1.3 VISIBLE AREA

This is transparent area without printed silver electrode or flexible print circuit printed with opaque ink, it assures quality clarified on specifications related to appearance standard.

8.1.4 NON ACTIVE AREA

Upper electrode or lower electrode of the non-active area is printed with transparent insulation ink; it is located in outside of the active area. Input by pen does not work in this area.

- Non active area is printed with insulation ink, hard push may cause transformation of upper electrode film, active area located near may contact together, may generate conductive power.
- Since a role of non-active area is to hold flatness of the upper electrode film on its structure, hard pushing by pen or on housing may cause functional error.

8.2 PRECAUTION ON DESIGNING PRINT CIRCUIT OR TOUCH PANEL

8.2.1. There is contact resistance between upper and lower electrode of the Touch Panel. Setting impedance of receiving circuit high enough on the design is recommended. Lower impedance may cause functional

DATA VISION 01/09/27 21 / 24

error.

- 8.2.2. Conduction between upper and lower electrode generates contact resistance. Data input by pen or finger should be started after the contact resistance become stable enough. Otherwise it may cause functional error.
- 8.2.3. Touch Panel picks up noise easily, any measures such as earth, etc. is recommended. Otherwise it may cause functional error.

8.3 PRECAUTION ON DESIGNING HOUSING

(Please sees drawing of housing assembly 2.)

8.3.1.TO RETAIN SPACE BETWEEN UPPER ELECTRODE FILM AND HOUSING TOP.

- Retain 0.2~0.8mm space above the non-active area not to make pressure on upper electrode film. If there is any pressure on it. It may cause functional error due to transformation of the upper electrode film.
- Flexible material such as robber is recommended for cushion materials. It should be fixed outside of visible area. If it is placed over non-active area, it may cause functional error due to transformation of the upper electrode film.

8.4 TO ASSEMBLE ON HOUSING

- To fix Touch Panel on Housing, supporting Touch Panel from backside (lower electrode glass) is recommended. If upper electrode film is fixed with both sides adhesive tape, it may lead to pooling off of the upper electrode film due to repeated input pressure.
- TO PREVENT SWELLIG OF UPPER ELECTRODE FILM OF TOUCH PANEL CAUSED BY ATMOSPHERIC PRESSURE DIFFERENCE BETWEEN INSIDE ND OUTSIDE OF THE DEVICE. ETC.
 - If upper electrode film swells caused by atmospheric pressure difference between inside and outside of the device, etc., it may cause deterioration of durability of Touch Panel and may cause functional error.
- TO PREVENT DEW CONDENSATION ON TOUCH PANEL AND TO PREVENT ANY LIQUID SUCH AS WATER. VAPOR FROM COMING INTO TOUCH SCREEN.

Upper electrode film and lower electrode glass of Touch Panel are fixed with adhesive, and they're set up a vent hole between them. This shows liquid may penetrate into Touch Panel easily due to its structure, any measures on designing the Housing to prevent the penetration is required. Penetration of liquid may cause functional error.

8.4 PRECAUTION ON UNPACKING AND ASSEMBLING TOUCH PANEL. 8.4.1.STORAGE

Store the product without unpacking a place where temperature and humidity is within the range clarified on specifications.

DATA VISION 01/09/27 22 / 24

8.4.2. UNPACKING

- Check upper and lower side and be sure to unpack from upper side.
- Be careful not to hit the product when any tool such as sharp knife is to be used for unpacking.
- Do not hold and pull out flexible tail, otherwise it may cause shut down of the flexible print circuit.
- Any treatment is not made for glass edge. It may be sharp and may cause any injury when handled by bare hands. Wear fingers tall or glove and handle with extra care.

8.4.3. HANDLING

- Pick up outside of visible area for handling. Do not pick up canter of the visible area and flexible tail.
- Do not stack up the products and do not place anything on the product. It may cause scratch or transformation.
- Wipe out any dirt on the product with dried flexible cloth. If it is heave dirt, wipe it out with flexible cloth with some ethyl alcohol. Upper electrode film and lower electrode glass of Touch Panel are fixed with adhesive, and they're set up a vent hole between them. Therefore ethyl alcohol may penetrate into Touch Panel easily from the edge, so extra care is required. It may cause functional error.

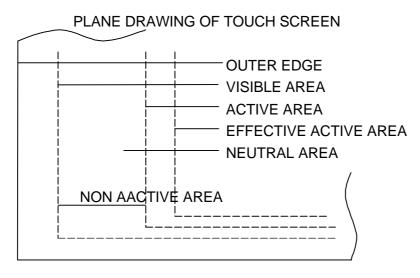
8.4.4. PRECAUTION ON ASSEMBLY

- Be careful not to generate excess distortion on heat sealed area and flexible tail. It may cause functional error.
- Be careful not to scratch the product on assembly.

8.4.5. PRECAUTION ON HANDLING

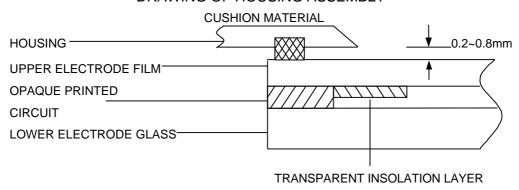
- Handle the product within the range of temperature and humidity clarified on specifications.
- Use finger or polyacetal pen attached for input to Touch Panel. Surface of the Touch Panel is bar-code treated, film surface may be damaged if inputted by ball-point pen or metal piece.
- Do not expose Touch Panel to direct sunlight for long period of time. Polyester film is used on Touch Panel, exposure to direct sunlight for long period of time may cause discoloration.
- If Chemical stays on the Touch Panel for long period of time, upper electrode film may be swelled and may cause functional error. If it is to be used under sever circumstances, another measures for water protection is required.
- 8.5 If any other question may be arise; please feel free to contact us.

DATA VISION 01/09/27 23 / 24



DRAWING 1

DRAWING OF HOUSING ASSEMBLY



DRAWING 2

DATA VISION 01/09/27 24 / 24